

REMARKS

Reexamination and reconsideration of this application as amended is requested. By this amendment, claims 1, 7, 10-12, and 15 have been amended. Claims 1-2 and 7-15 remain pending in this application. No new matter has been added to the claims.

The Present Invention

The present invention provides a more efficient method for the customization of gate delays that utilizes a VHDL package of array constants. The VHDL package of array constants replaces a significant amount of SDF file declarations for back annotation. The VHDL package of constants is efficient because it only has to be as large as the correlation of the delays, which can be quite significant when delay values are typically clustered around a range of values. Page 18, lines 9-10 of the instant specification. The back annotation process for the gate delays consists merely of resolving constant values for the fixed equations for the delay generics in the VHDL that describe gate behavior for the technology. These delay equations are formulated to depend on just two generics (rise/fall super generics) per gate instance. Page 28, lines 7-9 of the instant specification. The two generics the equations utilize are extracted via a SDF **which is significantly reduced in size**. Page 28, lines 3-6 of the instant specification. Therefore the back annotation process, which is a considerable space and time penalty for large chips in prior art (page 3, lines 12-18 of the instant specification), **is reduced to just two generic back annotations per gate instance**. The instant specification describes a VHDL library method that exploits these savings. Run time binding support of VHDL is utilized to have the constants in the VHDL delay equations resolved at model simulation time, which is a more efficient process than the traditional SDF back annotation of each individual gate delay value. Page 31, line 8-13 of the instant specification.

The instant method of customizing logic gate delays provides both space and time savings. For large chips, the SDF is typically the same size as, or larger than, the chip logic VHDL model, which imparts a huge overhead in storage and processing time in delay

customization of a chip during simulation. The correlation of delays (which is the claimed subject matter of co-pending application no. 10/038,209) affords significant savings in the number of delay values that must be specified. This enables innovation in the method defining those delays, as well as enabling innovation in the method to back annotate those delays to VHDL model.

In each of the references cited in the Office Action, the overhead of SDF lexical scan/parse, delay extraction, and application of delay to generic variables in the simulation model VHDL, is required for each individual delay defined in each gate instance. All of this data must be described in the SDF, which amounts to a huge amount of data for large chips.

The subject matter of the presently claimed invention utilizes a VHDL equation, where the equation resolves to a constant value, once all constants are resolved at simulation time. The annotation of just two generics per gate instance significantly reduces the processing time and space required for back annotation. The linear relationship of two generics per gate instance holds no matter what size chip is simulated. This allows chips to participate in simulation, which may not have been able to be simulated due to size limitations or performance concerns directly attributable to SDF processing. The instant specification discloses an embodiment of a VHDL library method to realize these savings. In summary, the claimed invention provides a method to customize a generic chip VHDL gate library with specific delay values in a more efficient manner (with significant space and processing time savings) than in the prior art.

Claims Rejection under 35 U.S.C. § 112, first paragraph

(14) The Examiner rejected Claim 10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner states that the specification does not reasonably provide enablement for “a storage medium” and that the term “processing medium” has no antecedent basis in the specification.

With regard to "a storage medium," Applicants respectfully traverse the Examiner's conclusion. Page 11, lines 20-23 of the specification of the instant application, for example, states: "The computer readable medium, for example, may include non-volatile memory, such as Floppy, ROM, Flash memory, disk drive memory, CD-ROM, and other permanent storage." Therefore, permanent storage is included in the definition of computer readable medium. It is therefore submitted that not only is "a storage medium" well known to those of normal skill in the art, it is also fully supported in the specification as originally filed.

With regard to the term "processing medium," Applicants are unable to find an instance of the term in claim 10. The term "processing circuit," however, does appear in claim 10. Applicants will assume that the Examiner's objection applies to this term instead. Accordingly, claim 10 has been amended to change the term "the processing circuit" to "a processing circuit."

It is therefore submitted that the rejection of claim 10 under 35 U.S.C. § 112, first paragraph, as discussed above, has been overcome. Applicants request that the Examiner withdraw the rejection of Claims 10.

Claims Rejection under 35 U.S.C. § 112, second paragraph

(15) The Examiner rejected claim 11 under 35 U.S.C. § 112, second paragraph, as failing to have antecedent basis in the claim from which it depends.

Accordingly, claim 11 has been amended to recite "the computer program product," which derives proper antecedent basis from claim 10, from which claim 11 depends.

In view of the amendment to claim 11, Applicants believe that the rejection of Claim 11 under 35 U.S.C. § 112, second paragraph, as discussed above, has been overcome. Applicants request that the Examiner withdraw the rejection of Claim 11.

Claim Rejections - 35 USC § 103

(16) The Examiner rejected Claims 1-2 and 10-14 under 35 U.S.C. 103(a) as being unpatentable over IEEE Standard for VITAL ASIC Modeling Specification—IEE Std 1076.4-1995 (Std1076 hereafter), in view of Standard Delay Format Specification Version 2.1 by Open Verilog International (OVI2.1 hereafter).

Amended claims 1 and 10 recite, *inter alia*:

Storing in a memory a tpd_super_rise generic declaration and a tpd_super_fall generic declaration for every VHDL gate model in a VHDL technology library;

initializing other generic variables, each derived solely from at least one of the tpd_super_rise generic declaration and the tpd_super_fall generic declaration, corresponding to every VHDL gate model in the VHDL technology library to an equation representing a correlation policy; and

storing in a memory an updated VHDL technology library including the tpd_super_rise generic declaration and the tpd_super_fall generic declaration for every VHDL gate model, and the initialized other generic variables.

The instant application is one of three related applications. The two other related applications address the analysis and representation of chip gate delays, and associated generics, to realize a much reduced representation of SDF (Standard Delay Format file) timing information, such that a particular delay generic is not bound to a particular gate instance, which ~~now allows the sharing of a particular delay value amongst many gate instances. The novel~~ library structure, method, and system, of the present invention to accommodate the requirements efficiently represents the data while being compatible with the inventions of the other two related patent applications in a design process.

Support for the amendment to claims 1 and 10 is found on page 32 and page 33 of the specification as originally filed. Page 32 shows an example of actual library text required to customize a AND2_H gate in a library for the 1X type data structure (where 1X type is a "correlation policy" as specified in claims 1 and 10). Page 33 of the instant specification shows

Page 10 of 15

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an example of the actual text required to customize an AND2_H gate in a library for the 2X type date structure (or policy). Specifically, with reference to claims 1 and 10, on page 32 the two super generics are defined Tpd_super_rise and Tpd_super_fall of type STRING. In contrast with the prior art, the present invention only uses two super_generics (*Storing in a memory a tpd_super_rise generic declaration and a tpd_super_fall generic declaration for every VHDL gate model in a VHDL technology library*). One can see that a string of characters is all that is needed to customize the other generic values, since the following equation is only a function of elements in the super generics. The following equation actually maps a specific delay value to the first pin (Tpd_a) of the gate as an example of how "other generic values" are initialized in amended claims 1 and 10. The left hand side of the equation (before "!=" sign), Tpd_a : VitalDelayType01, is IEEE standard notation for specification of a generic variable. The right hand side of the "!=" introduces an equation that is unique to the present invention.

The equation is of a format $var = (rise, fall)$, where rise and fall are some terms that are derived based on an element of the super generics, in this case its Tpd_super_rise(0) and Tpd_super_fall(0), respectively. The format of the equation is a function of the technology policy as explained on page 33 of the specification.

Page 32 describes a 2X structure (or policy). In this case super generic element 1 is utilized to index into an array of constants to get the actual delay value. The actual array constants are supplied at run time via the late binding feature of VHDL (prior art).

Ultimately, a library customization method is claimed that relies on just two generics, with a unique mechanism for deriving the actual generic values (*initializing other generic variables, each derived solely from at least one of the tpd_super_rise generic declaration and the tpd_super_fall generic declaration*), which are typically much more in number. The claimed method: 1) eliminates the need to define all of the generics in an SDF for each gate instance (e.g. multiply number of generics by number of gate instances, which are easily in the thousands for any reasonably sized chip); and 2) eliminates the back-annotation process of finding the matching gate instance in SDF and transferring the unique value to each unique instance of the gate.

The 1076 reference utilizes generics to back annotate timing data. However, the 1076 reference discloses a typical one-to-one mapping of generic values in the technology library to a particular gate instance; such that the back annotation is straight forward, but very time consuming, considering the number of gates (e.g. 100,000 instances of AND gate, 200,000 instances of inverter etc). The 1076 reference does not declare "a *tpd_super_rise* generic declaration and a *tpd_super_fall* generic...for every VHDL gate model in a VHDL technology library," as recited in claims 1 and 10 of the instant application.

Additionally, neither the 1076 reference nor the OVI2.1 reference disclose *initializing other generic variables, each derived solely from at least one of the tpd_super_rise generic declaration and the tpd_super_fall generic declaration*, as recited in amended claims 1 and 10 of the instant application.

Claim 12 has been amended to contain limitations similar to claims 1 and 10, and, therefore, distinguishes over the art for the same reasons claims 1 and 10 distinguish over the prior art.

Accordingly, in view of the remarks above, since neither the Std1076, the OVI2.1, nor any combination of the two cited references, teaches, anticipates, or suggests, the presently claimed correlation policy, Applicants believe that the rejection of Claims 1-2 and 10-14 under 35 U.S.C. 103(a) has been overcome. The Examiner should withdraw the rejection of these claims.

(17) The Examiner rejected Claim 15 under 35 U.S.C. 103(a) as being unpatentable over IEEE Standard for VITAL ASIC Modeling Specification—IEE Std 1076.4-1995 (Std1076 hereafter), in view of IEEE Standard for Integrated Circuit (IC) Delay and Power Calculation System—IEEE Std 1481-1999 (Std1481 hereafter). Claim 15 has been amended.

Claim 15 recites, *inter alia*:

using a *tpd_super_rise* generic declaration and a *tpd_super_fall* generic

declaration, each generic declaration comprising at least one pointer, for every VHDL gate model in a VHDL technology library to index into a 3-dimensional variable data array structure comprising delay values, wherein the VHDL technology library includes:

- one or more VHDL gate models;
- a `tpd_super_rise` generic declaration and a `tpd_super_fall` generic declaration for every VHDL gate model in the VHDL technology library;
- and

- one or more other generic variables, each derived solely from at least one of the `tpd_super_rise` generic declaration and the `tpd_super_fall` generic declaration, corresponding to every VHDL gate model in the VHDL technology library initialized to an equation representing a correlation policy...

Independent claim 15 has been amended to contain limitations consistent with independent claims 1, 10, and 12, as explained in the preceding section. Therefore, independent claim 15 distinguishes over the art for the same reasons claims 1, 10, and 12 distinguish over the prior art.

Accordingly, in view of the remarks above, since neither the Std1076, Std 1481, nor any combination of the two cited references, teaches, anticipates, or suggests, the presently claimed generic variables derived solely from at least one of the `tpd_super_rise` generic declaration and the `tpd_super_fall` generic declaration, Applicants believe that the rejection of Claim 15 under 35 U.S.C. 103(a) has been overcome. The Examiner should withdraw the rejection of this claim.

(18) The Examiner rejected Claim 7 under 35 U.S.C. 103(a) as being unpatentable over IEEE Standard for VITAL ASIC Modeling Specification—IEE Std 1076.4-1995 (Std1076 hereafter), in view of IEEE Standard for Integrated Circuit (IC) Delay and Power Calculation System—IEEE Std 1481-1999 (Std1481 hereafter), further in view of Standard Delay Format Specification Version 2.1 by Open Verilog International (OVI2.1 hereafter). Claim 7 has been amended.

Claim 7 recites, *inter alia*:

inserting a tpd_super_rise generic declaration and a tpd_super_fall generic declaration for at least one VHDL gate model in the VHDL technology library; initializing other generic variables, each derived solely from at least one of the tpd_super_rise generic declaration and the tpd_super_fall generic declaration, in every VHDL gate model in the VHDL technology library to an equation representing a correlation policy...

Independent claim 7 has been amended to contain limitations consistent with independent claims 1, 10, 12, and 15, as explained in the preceding sections. Therefore, independent claim 7 distinguishes over the art for the same reasons claims 1, 10, 12, and 15 distinguish over the prior art.

Accordingly, in view of the remarks above, since neither the Std1076, the OVI2.1, or the STD1481, nor any combination of the three cited references, teaches, anticipates, or suggests, the presently claimed generic variables derived solely from at least one of the tpd_super_rise generic declaration and the tpd_super_fall generic declaration, Applicants believe that the rejection of Claim 7 under 35 U.S.C. 103(a) has been overcome. The Examiner should withdraw the rejection of this claim.

Conclusion

The foregoing is submitted as full and complete response to the Official Action mailed January 4, 2006, and it is submitted that Claims 1-2 and 7-15 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of Claims 1-2 and 7-15 is earnestly solicited.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants acknowledge the continuing duty of candor and good faith to disclose information known to be material to the examination of this application. In accordance with 37 CFR § 1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and the attorneys.

If the Examiner believes that there are any informalities that can be corrected by Examiner's amendment, or that in any way it would help expedite the prosecution of the patent application, a telephone call to the undersigned at (561) 989-9811 is respectfully solicited.


The Commissioner is hereby authorized to charge any fees that may be required or credit any overpayment to Deposit Account 50-1556.

In view of the preceding discussion, it is submitted that the claims are in condition for allowance. Reconsideration and re-examination is requested.

Respectfully submitted,

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